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EXAMINER	
NGUYEN, DANG T	
ART UNIT	**PAPER NUMBER**
2824	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/600,065	SHIEH ET AL.	
	Examiner	Art Unit	
	Dang T. Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/5/07 of Applicant's Amendment*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-10,12-24,26 and 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-10,12-24,26 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Amendment

1. This office action is in response to Applicant's amendment received on 4/5/07.

2. Claims 1, 13, 17 and 24 have been amended. Claims 5, 11 and 25 have been cancelled. Claims 1 – 4, 6 – 10, 12 – 24, 26 and 27 are pending on this application. Claims 1, 13, 17 and 24 are independent claims.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 – 4, 6 – 10, 12 - 14, 17 – 24 and 26, are rejected under 35 U.S.C. 102(e) as being anticipated by Van Buskirk et al., Pub. No.: US 2003/0208663 A1 - filed May 1, 2002.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding independent claim 1, Figs. 9 and 10 of Van Buskirk disclose an architecture that facilitates a reference voltage in a multi-bit memory (302), comprising: a multi-bit memory core (210) including a plurality of data cells (200) for storing data; first and second reference arrays (Dynamic Reference A, Dynamic Reference B) fabricated adjacent to each other (Figs. 9 and 2 for disclosing reference A and B adjacent to each other, see Page 6, paragraph 0050 lines 10 -12) and associated with one of a plurality of sectors (Fig. 10 for disclosing associated with one of a plurality of sectors, Page 6, paragraph 0050, lines 3 – 11) comprising multi-bit data cells (Page 6, paragraph 0049 lines 2 – 6), the first and second reference arrays (Dynamic Reference A, Dynamic Reference B) each comprises of a plurality of multi-bit reference cells (202's of Reference A, 204's of Reference B) fabricated on the memory core (210 Fig. 10), wherein reference cells (202s) within the first reference array (Reference A) have a first voltage level and reference cells (204s) within the second reference array (Reference B) have a second voltage level, the second voltage level different than the first voltage level (Van Buskirk does not clearly disclose the second voltage level of the second reference array different than the first voltage level of the first reference array. However, It must be used two different voltages to form an average as disclosed in fig. 5; since if two voltages are the same then can not do an average for example: If the first voltage is 5V and second voltage is 5V then the average is 5V. Therefore, the voltages of those two levels must be different).

a first bit value (NB Fig. 5) of a first reference cell (94 Fig. 5) of the first reference array (Ref A Fig. 5) averaged with a second bit value (NB Fig. 5) of a second reference

cell (96 Fig. 5) of the second reference array (Ref B Fig. 5) to arrive at the reference voltage (Fig. 5 (A+B)/2) employed during a data cell read operation (Page 4, paragraph 0041 line 9).

Regarding dependent claims 2 and 18, Figs. 9 and 10 of Van Buskirk disclose the core (210) further comprising a sector (Sector 1) of multi-bit data cells (200) organized in rows and columns with associated word lines (WLs) attached to the multi-bit data cells (200) in a row and with associated bit lines (BLs) attached to the multi-bit data cells (200) in a column, the first and second reference cells (202, 204) forming a multi-bit reference pair (REFERENCE A and REFERENCE B) that is programmed and erased with the multi-bit data cells (200) during programming and erase cycles (Page 7, paragraph 0052).

Regarding dependent claims 3 and 19, Fig. 8 of Van Buskirk discloses that the multi-bit reference pair (202, 204) is associated with a word in a word line (WL0), the multi-bit reference pair (REFERENCE A and REFERENCE B) utilized during reading of bits of the word (Page 6, paragraph 0047).

Regarding dependent claims 4 and 20, Figs. 9 and 10 of Van Buskirk disclose that the multi-bit reference pair (202, 204) is associated with multi-bit data cells (200) in a wordline (WL0), the multi-bit reference pair (202 and 204) is utilized during reading of bits in the wordline (Page 4, paragraph 0041, line 9).

Regarding dependent claims 6 and 22, Figs. 9 and 10 of Van Buskirk further disclose that the multi-bit reference pair (202 and 204) is associated with multi-bit data

cells (200) in the sector (Sector 1), the multi-bit reference pair (202, 204) is utilized during reading of bits in the sector (Page 6, paragraph [0050).

Regarding dependent claims 7 and 23, Figs. 9 and 10 of Van Buskirk discloses that the memory core (210) includes a plurality of data sectors (Sector 1 and Sector 2) that are accessible by the first and second reference arrays (REFERENCE A and REFERENCE B), the first and second reference arrays (REFERENCE A and REFERENCE B) are located centrally of the plurality of data sectors (Sector 1 and Sector 2).

Regarding dependent claim 8, Van Buskirk discloses an integrated circuit comprising the memory (Page 7 claim 13).

Regarding dependent claim 9, Van Buskirk discloses a memory core of a computer system (Page 7 claim 14).

Regarding dependent claim 10, Van Buskirk discloses an electronic device comprising the memory (Page 7 claim 15).

Regarding dependent claims 12 and 26, Figs. 9 and 10 of Van Buskirk discloses the memory core (210) further comprising a plurality of data sectors (Sector 1 and Sector 2) such that each data sector is associated with at least one of the first and second reference array (REFERENCE A and REFERNCE B) of multi-bit reference cells (202 and 204).

Regarding independent claim 13, Figs. 9 and 10 of Van Buskirk disclose an architecture that facilitates a reference voltage in a multi-bit memory comprising: a multi-bit memory core (210) for storing data, the memory core including two groups of data

sectors (Sector 1 and Sector 2); first and second reference arrays (REFERENCE A and REFERENCE B) fabricated adjacent to each other (Figs. 9 and 2 for disclosing reference A and B adjacent to each other, see Page 6, paragraph 0050 lines 10 -12) and associated with one of the two groups of data sectors (Fig. 10 for disclosing associated with one of a plurality of sectors, Page 6, paragraph 0050, lines 3 – 11) comprising multi-bit data cells (Page 6, paragraph 0049 lines 2 – 6), the first and second reference arrays (Reference A and Reference B) each comprised of a plurality of multi-bit reference cells (202's of Reference A, 204's of Reference B), fabricated on the memory core (210) interstitial to the groups of data sectors (Sector 1 and Sector 2), wherein reference cells (202s) within the first reference array (Reference A) have a first fixed voltage level; and reference cells (204s) within the second reference array (Reference B) have a second distinct fixed voltage level (Van Buskirk does not clearly disclose the second voltage level of the second reference array different than the first voltage level of the first reference array. However, It must be used two different voltages to form an average as disclosed in fig. 5; since if two voltages are the same then can not do an average. F or example: If the first voltage is 5V and the second voltage is 5V then the average is 5V. Therefore, the voltages of those two levels must be different); and

a first bit value (NB Fig. 5) of a first reference cell (94 Fig. 5) of the first reference array (REF. A) and a second bit value (NB Fig. 5) of a second reference cell (96 fig. 5) of the second reference array (REF. B Fig. 5) forming a reference pair whose respective

bit values are averaged ((A+B)/2 Fig. 5) to arrive at the reference voltage for the read operation (Page 4, paragraph 0041 line 9).

Regarding dependent claim 14, Van Buskirk discloses the groups of data sectors read in an interleaved manner with a selected reference pair (Page 6 paragraph 0048).

Regarding independent claim 17, Fig. 9 and 10 of Van buskirk disclose a method for providing a reference voltage in a multi-bit memory, comprising: receiving a multi-bit memory core (210) for storing data; providing first a and second reference arrays (Reference A and Reference B) fabricated adjacent to each other (Figs. 9 and 2 *for disclosing reference A and B adjacent to each other*, see Page 6, paragraph 0050 lines 10 -12) and associated with one of a plurality of sectors (Fig. 10 *for disclosing associated with one of a plurality of sectors*, Page 6, paragraph 0050, lines 3 – 11), comprising multi-bit data cells (Page 6, paragraph 0049 lines 2 – 6), the first and second reference arrays (Reference A and Reference B) each comprised of a plurality of multi-bit reference cells (202s and 204s) fabricated on the memory core (210), the first and second reference arrays (Reference A and Reference B) including corresponding reference cells that are interweaved among data cells in the multi-bit memory core, wherein reference cells within the first reference array have a first voltage level and reference cells within the second reference array have a second disparate voltage level (Van Buskirk does not clearly disclose wherein reference cells within the first reference array have a first voltage level and reference cells within the second reference array have a second disparate voltage level. However, It must be used two disparate voltages

to form an average as disclosed in fig. 5; since if two voltages are the same then can not do an average for example: If the first voltage is 5V and the second voltage is 5V then the average is 5V. Therefore, the voltages of those two levels must be different); and

Averaging a first bit value (NB Fig. 5) of a first reference cell (94 Fig. 5) of the first reference array (Ref. A) with a second bit value (NB Fig. 5) of a second reference cell (96 Fig. 5) of the second reference array (Ref. B) to arrive at the reference voltage (Fig. 5, (A+B)/2) utilized during a data cell read operation (Page 4, paragraph 0041 line 9).

Regarding dependent claim 21, Fig. 8 of Van Buskirk discloses the method of claim 18, as discussed above, the associated multi-bit reference pair (202, 204) utilized during reading of bits in the corresponding word line (Page 6, paragraph 0047).

Regarding independent claim 24, Figs. 9 and 10 of Van Buskirk disclose a system for providing a reference voltage in a multi-bit memory, comprising: means for providing a multi-bit memory core (210) for storing data; means for providing first and second reference arrays (Reference A and Reference B) fabricated adjacent to each other (Figs. 9 and 2 *for disclosing reference A and B adjacent to each other*, see Page 6, paragraph 0050 lines 10 -12) and associated with one of a plurality of sectors comprising multi-bit data cells, the first and second reference arrays each comprises of a plurality of multi-bit reference cells (202s and 204s), the first and second reference arrays (Reference A and Reference B) including corresponding reference cells (202s and 204s) that are interweaved among data cells (Page 6, paragraph 0048 lines 10-11) within the multi-bit memory core (210), the first and second reference arrays (Ref. A and

Ref. B) fabricated on the memory core (210), wherein reference cells (202s) within the first reference array (Reference A) comprise a first fixed voltage level and reference cells (204s) within the second reference array (Reference B) comprise a second disparate fixed voltage level (Van Buskirk does not clearly disclose wherein reference cells within the first reference array comprise a first fixed voltage level and reference cells within the second reference array comprise a second disparate fixed voltage level. However, It must be used two disparate voltages to form an average as disclosed in fig. 5; since if two voltages are the same then can not do an average for example: If the first voltage is 5V and the second voltage is 5V then the average is 5V. Therefore, the voltages of those two levels must be different); and

means for averaging (Fig. 5 (A+B)/2) a first bit value (NB Fig. 5) of a first reference cell (94 Fig. 5) of the first reference array (Ref A) with a second bit value (NB fig. 5) of a second reference cell (96 Fig. 5) of the second reference array (Ref B) to arrive at the reference voltage (Fig. 5, (A+B)/2) to facilitate a read operation (Page 4, Paragraph 0041, line 9).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Van Buskirk et al., Pub. No.: US 2003/0208663 view of Ferrant, Patent No. US 6,538,942 B2 - filed Jun. 18, 2001.

Regarding dependent claim 15, Van buskirk as applied to claim 13 above discloses every aspect of applicant's claimed invention except for the first and second reference arrays being precharged before being averaged.

Ferrant discloses precharging a row of reference cells. Ferrant teaches that the use of precharge circuit for precharging the reference cells before a reading or comparing operation is well known in the memory art (as shown in col. 1 lines 47-49).

Van Buskirk and Ferrant are both related to memory cells. In view of Ferrant, it would have been obvious to one having ordinary skill in the art at the time the invention was made to precharge the reference arrays of Van Buskirk before averaging for the purpose of improving the accuracy of average operation.

5. Claims 16 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Buskirk et al., Pub. No.: US 2003/0208663 in view of Kurihara et al., U.S. Patent No. US 6,791,880 B1 - filed May 6, 2003.

Regarding dependent claims 16 and 27, Van buskirk as applied to claims 13 and 24 above, respectively, discloses every aspect of applicant's claimed invention except for a redundancy array located at least one of proximate and adjacent to the groups of data sectors.

Fig. 5 of Kurihara discloses a redundancy [525] array located at least one of proximate and adjacent to the groups of data sectors.

Van Buskirk and Kurihara are both related to multi-bit memory cells. In view of teaching of Kurihara, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate Kurihara's redundancy into the memory core of Van Buskirk for the purpose of providing optimum tracking of the reference memory cells and core memory cells (Col. 6 lines 8-9).

Response to Arguments

6. Applicant's arguments 1/31/06 have been fully considered but they are not persuasive.

Under remarks, with respect to claims 1, 13, 15-17, 24 and 27, applicant argued that Van Buskirk does not disclose "the first and second reference arrays each comprised of a plurality of multi-bit reference cells fabricated on the memory core, wherein reference cells within the first reference array have a first voltage level and reference cells within the second reference array have a second voltage level, the second voltage level different than the first voltage level". Examiner respectful disagrees for the following reasons:

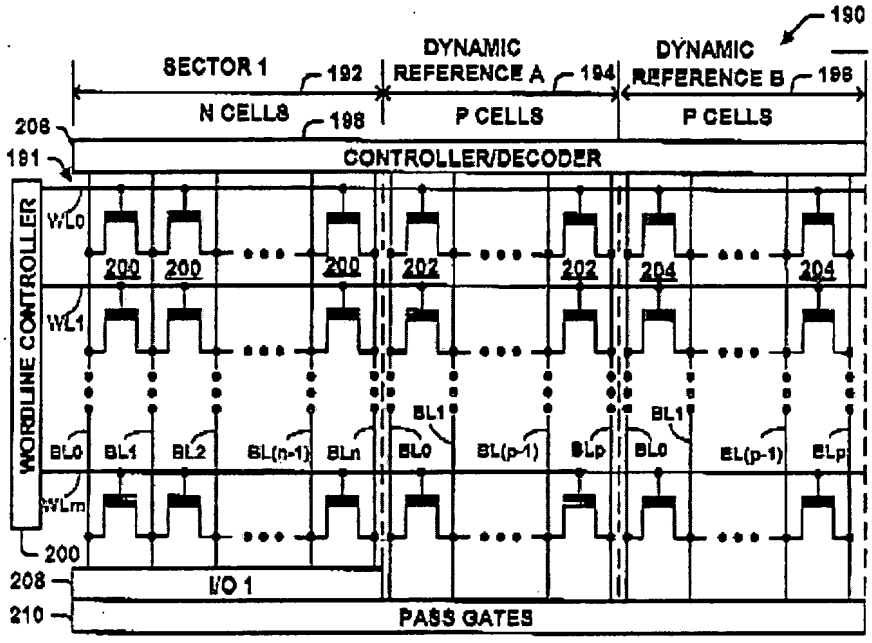

FIG. 9

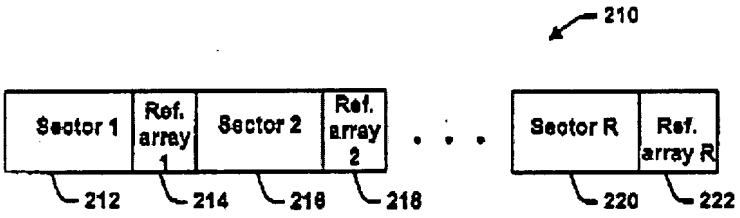

FIG. 10

Figs. 9 and 10 of Van Buskirk above disclose the first (Ref. A) and second (Ref. B) reference arrays each comprised of a plurality of multi-bit reference cells (202s and 204s) fabricated on the memory core (210 Fig. 10), Van Buskirk does not clearly disclose wherein reference cells within the first reference array have a first voltage level and reference cells within the second reference array have a second disparate voltage level. However, It must be used two disparate voltages to form an average as disclosed

in fig. 5; since if two voltages are the same then can not do an average for example: If the first voltage is 5V and second voltage is 5V then the average is 5V. Therefore, the voltages of those two levels must be different.

Per explained above, the prior art from previous office action is applying to this office action.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

8. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.

Dang Nguyen 6/11/2007

ANH PHUNG
PRIMARY EXAMINER